

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1        1.    (Currently Amended) A computer implemented method of  
2    multilevel dither screening comprising the steps of:  
3        defining a dither value for each pixel of a screening matrix;  
4        packing plural pixel values corresponding to plural pixels  
5    into equal sections of a first data word;  
6        packing plural corresponding dither values into ~~said~~ equal  
7    sections of a second data word, said equal sections of said second  
8    data word identical to said equal sections of said first data word;  
9        adding corresponding sections of said first data word and said  
10   second data word in an arithmetic logic unit selectively spilttable  
11   into ~~said~~ equal sections corresponding to said equal sections of  
12   said first and second data words thereby forming a sum data word;  
13        saturating any section of said sum data word ~~generating that~~  
14   has generated a carry output during said adding to form a  
15   corresponding section of all 1's and passing other sections  
16   unchanged thereby forming a saturated sum data word; and  
17        truncating a predetermined number of least significant bits of  
18   each section of said saturated sum data word thereby forming a  
19   dither screen data word.

1        2.    (Currently Amended) The method of claim 1, wherein:  
2        said step of adding corresponding sections said first data  
3    word and said second data word further includes saving a carry out  
4    of each section in a multiple flags data word;  
5        said step of saturating any section of said sum data word  
6    ~~generating an~~ that has generated a carry output during addition  
7    includes

8           expanding said carry out of each section in said multiple  
9       flags data word to fill a corresponding section of a mask data  
10      word,

11           forming the logical OR of (1) a logical AND of a  
12      saturated data word having all 1's in every section and said  
13      mask data word, and (2) a logical AND of said sum data word  
14      and a logical inverse of said mask data word.

1       3. (Currently Amended) The method of claim 1, wherein:  
2       said step of truncating a predetermined number of least  
3      significant bits of each section of said saturated sum data word  
4      includes

5           right shifting said saturated sum data word ~~said~~  
6      predetermined a number of bits equal to said predetermined  
7      number of least significant bits of each section,

8           forming a mask data word having ~~said predetermined~~ a  
9      number of 1's in least significant bits of each section equal  
10     to said predetermined number of least significant bits of each  
11     section and 0's in most significant bits of each section, and

12           forming a logical AND of said right shifted saturated sum  
13      data word and said mask data word.

1       4. (Currently Amended) The method of claim 1, wherein:  
2       said ~~input~~ pixel values are represented in a fixed point  
3      format of 8 bits including 4 integer bits and 4 fractional bits;  
4       said dither values are represented in a fixed point format of  
5      4 bits including zero integer bits and 4 fractional bits; and  
6       said predetermined number of least significant bits of said  
7      step of truncating is 4.

1       5. (Original) The method of claim 1, further comprising the  
2      step of:

3 quantizing each section of said dither screen data word into a  
4 limited set of threshold ranges.

1 6. (Currently Amended) A printer comprising:

2 a transceiver adapted for bidirectional communication with a  
3 communications channel;

4 a memory;

5 a print engine adapted for placing color dots on a printed  
6 page according to received image data and control signals; and

7 a programmable data processor connected to said transceiver,  
8 said memory and said print engine, said programmable data processor  
9 including a selectively splittable arithmetic logic unit, said  
10 programmable data processor programmed to:

11 receive print data corresponding to pages to be printed  
12 from the communications channel via said transceiver;

13 convert said print data into image data and control  
14 signals for supply to said print engine for printing a  
15 corresponding page, said conversion including multilevel  
16 dither screening by

17 defining a dither value for each pixel of a screening  
18 matrix,

19 packing plural pixel values corresponding to plural  
20 pixels into equal sections of a first data word,

21 packing plural corresponding dither values into ~~said~~  
22 equal sections of a second data word, said equal sections of  
23 said second data word identical to said equal sections of said  
24 first data word,

25 adding corresponding sections of said first data word and  
26 said second data word in said arithmetic logic selectively  
27 spilt into ~~said~~ equal sections corresponding to said equal  
28 sections of said first and second data words thereby forming a  
29 sum data word,

30 saturating any section of said sum data word ~~generating~~  
31 that has generated a carry output during said adding to a  
32 corresponding section of all 1's and passing other sections  
33 unchanged thereby forming a saturated sum data word; and  
34 truncating a predetermined number of least significant  
35 bits of each section of said saturated sum data word thereby  
36 forming a dither screen data word.

1 7. (Currently Amended) The printer of claim 6, wherein:  
2 said programmable data processor further including  
3 a multiple flags register connected to said arithmetic  
4 logic unit receiving and storing a carry out from each of said  
5 sections of said arithmetic logic unit, and  
6 an expand circuit connected to said multiple flags  
7 register for expanding each bit of said multiple flags  
8 register to fill a corresponding section thereby forming a  
9 mask data word; and  
10 wherein said programmable data processor is programmed to saturate  
11 any section of said sum data word ~~generating an~~ that has generated  
12 carry output during addition by  
13 forming in said arithmetic logic unit the logical OR of  
14 (1) a logical AND of a saturated data word having all 1's in  
15 every section and said mask data word, and (2) a logical AND  
16 of said sum data word and a logical inverse of said mask data  
17 word.

1 8. (Currently Amended) The printer of claim 6, wherein:  
2 said programmable data processor further including  
3 a selectable shifter,  
4 a mask generator having an input and an output, said mask  
5 generator forming a mask data word having filling each section

6        filled with a number of least significant 1's equal to a  
7        number received at said input, and  
8        wherein said programmable data processor is programmed for  
9        truncating a predetermined number of least significant bits of each  
10       section of said saturated sum data word by  
11           supplying said predetermined number to said shifter to  
12       right shift said saturated sum data word by said predetermined  
13       number of bits,  
14           supplying said predetermined number to said input of said  
15       mask generator thereby forming a mask data word having said  
16       predetermined number of 1's in least significant bits of each  
17       section and 0's in most significant bits of each section, and  
18           forming in said arithmetic logic unit a logical AND of  
19       said right shifted saturated sum data word and said mask data  
20       word.